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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,588	01/15/2004	Hajime Akimoto	HITA.0488	4908

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,588	AKIMOTO ET AL.	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-24 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-10, 12-24 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, March 12th, 2009 the Applicant amended claims 1, 3-10, 12, cancelled claims 2, 11 and added new claims 32-33. Currently claims 1, 3-10, 12-24 and 29-33 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 12th, 2009 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-24 and 29-33 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. Claim 1 is objected to because of the following informalities: the last line of the claim states, “the sate wiring forms the capacitance.” This appears to be a typo and the Applicants intended the phrase to read ‘the gate wiring forms the capacitance.” Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-4, 6-7, 9, 12-15, 17-18, 20, 23-24 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Yamazaki et al. (US 6,417,896) and further in view of Stewart et al. (US 5,952,789).

With respect to claim 1, Akimoto discloses, an image display device (fig. 1), comprising:

a display part configured by a plurality of pixels (clear from fig. 1) each having an electro-luminescent element driven to illuminate according to a display signal voltage Vs (7 in fig. 1) and said pixels being disposed in a matrix (161 in fig. 2);

a signal line (17 in fig. 1) used to write said display signal voltage in said pixel (see write period in fig. 2) and located in a direction of a column of the matrix (fig. 1);

a pixel selector (22 in fig. 1) for selecting a pixel from said plurality of pixels so as to write said display signal voltage therein through said signal line;

a display signal voltage generator (21 in fig. 1) for generating said display signal voltage;

an illuminating state controller (32, 9 in fig. 1) for controlling a selection of an illuminating state or non-illuminating state for each of said plurality of pixels at a time;

wherein one end of said electro-luminescent element provided in each said pixel is connected to a common power supply (common terminal connected to the element in fig. 1; also see end of para. 51) while the other end of said electro-luminescent element is selectively connected to a first source/drain electrode of an electro-luminescent

element driving transistor (4 in fig. 1) through a first switch (9 in fig. 1) said transistor has a threshold voltage Vth,

a second source/drain electrode of said electro-luminescent element driving transistor is connected to a power supply line applied with a prescribed voltage (18 in fig. 1; para. 43), and

the gate of said electro-luminescent element driving transistor (4 in fig. 1) is connected to the signal line through a capacitance (2 in fig. 1) and selectively connected to the first source/drain electrode of said electro-luminescent element driving transistor through a second switch (5 in fig. 1), and

when said illuminating state is selected, the first switch is fixed as ON, the second switch is fixed as OFF (see the waveforms for the light-on period in fig. 3), and a voltage that is lower than said prescribed voltage appears at the gate of said transistor (col. 6, lines 8-45),

a gate wiring forming the gate of said transistor is connected to the signal line directly through a capacitor element (fig. 1).

Akimoto does not expressly disclose an overlap between the signal line and the gate wiring.

Yamazaki discloses a pixel electrode (213 in figs. 5c and 7) wiring (input of 213 in fig. 7; and 213 in fig. 5c) that extends in the direction of the rows of the pixel matrix so as to overlap the gate line (207 in figs. 5c and 7), and

an overlap between the gate line and the pixel electrode wiring forms the capacitance (col. 9, lines 13-19).

Yamazaki and Akimoto are analogous art because they are both from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to align an extended portion of the gate wiring of the transistor of Akimoto in the same direction as the signal line, as taught by Yamazaki, to form the capacitance.

The motivation for doing so would have been to form a capacitor without reducing an aperture ratio and thereby improve the integration of the circuit (Yamazaki; col. 9, lines 17-20).

To further explain Yamazaki's circuit while different from that of Akimoto is certainly applicable. Yamazaki's pixel circuit calls for a pixel electrode connected to a gate line solely through a capacitor. Akimoto's circuitry calls for a gate electrode of a transistor connected to a data line solely through a capacitor. Yamazaki creates that capacitor by extending the pixel electrode to overlap the gate line. Thus it seems obvious that Akimoto's gate electrode should be extended along to overlap the data line.

Akimoto further discloses, a constant voltage supply, as evidenced by the signal line data during the write period in figure three. During an illumination period, Akimoto supplies a triangular signal amplitude as seen in figure three.

Akimoto does not expressly disclose supplying a constant voltage to each pixel during the illuminating state or that the constant voltage is lower than the prescribed voltage.

Stewart discloses, an image display device having an electro-luminescent element pixel circuit (610 in fig. 6; for example), wherein a constant voltage supply provides a constant voltage Vil (ground in fig. 4) to each of said plurality of pixels through said signal line (data line in fig. 6; D2 in fig 4) when said illuminating state is selected for a selected pixel (L1 in fig. 4; col. 6, lines 48-54), and that the constant voltage, Vil lower than said display signal voltage Vs (col. 6, lines 24-34) is applied to the signal line.

Stewart, Yamazaki and Akimoto are analogous art because they are both from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the triangular signal amplitude of Akimoto with the constant supply voltage of Stewart.

The motivation for doing so would have been to ensure a high display quality over time (Stewart; col. 2, lines 1-4)

With respect to claim 3, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein said first source/drain electrode is a drain electrode and said second source/drain electrode is a source electrode (para. 43).

With respect to claim 4, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is a p-channel transistor (fig. 4; also see para. 62).

With respect to claim 6, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is a polycrystalline silicon thin film transistor (para. 43).

With respect to claim 7, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is an n-channel transistor (fig. 6; also see para. 69).

With respect to claim 9, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto fails to disclose the use of amorphous silicon thin film transistors.

Stewart further discloses, the use of amorphous silicon thin film transistors (col. 6, lines 65-67).

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the transistors of Akimoto with the amorphous silicon thin film transistors of Stewart.

The motivation for doing so would have been the well known in the art advantage that amorphous silicon thin film transistors are more uniform over large areas than polycrystalline silicon thin film transistors.

With respect to claim 12, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein said electro-luminescent element driving transistor is actually driving in a sub-threshold area in which its gate-source voltage is a threshold voltage and under (para. 47).

With respect to claim 13, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto, when combined with Stewart further discloses, wherein one end of the signal line is connected to the display signal voltage generator and a constant voltage generator (Stewart; T8 in fig. 4) through a third switch (Akimoto; 23 in fig. 1; clear from fig. 1, that the signal line [17] is connected to the display signal voltage generator [21]).

With respect to claims 14-15, 17-18, 20 and 23, as these claims are identical to previously rejected claims 3-4, 6-7, 9 and 12, respectively, these claims are rejected on the same merits shown above.

With respect to claim 24, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein selection of said illuminating/non-illuminating state is repeated in each frame period (clear from fig. 21, that the operation repeats indefinitely).

With respect to claim 29, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto, when combined with Stewart, discloses, wherein when said illuminating state is selected said voltage appearing at the gate of said transistor is lower than said prescribed voltage by (Vs-Vil +|Vth|) (Akimoto's pixel circuit is identical to circuits presented by the Applicant, and furthermore Akimoto's disclosure details very similar operation to the current application (see col. 5, line 62 - col. 6, line 15). Therefore the voltage limitation on the gate of said transistor is seen as inherent in the operation of the pixel circuit disclosed by Akimoto).

With respect to claim 30, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 29 (see above).

Akimoto, when combined with Stewart, further discloses wherein when said illuminating state is selected, said electro-luminescent element is driven to by a voltage of (Vs-Vil) to illuminate (Akimoto; col. 6, lines 38-42).

With respect to claim 31, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 29 (see above).

Akimoto, when combined with Stewart, further discloses wherein the constant voltage Vil applied to the signal line is the lowest level of said display signal voltage Vs (Stewart; col. 6, lines 24-37).

7. Claims 5, 8, 16, 19 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Yamazaki et al. (US 6,417,896), Stewart et al. (US 5,952,789) and further in view of Misawa et al. (US 5,250,931).

With respect to claim 5, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is configured as a p-channel transistor (see fig. 4; para. 62).

Neither Akimoto nor Stewart expressly disclose, that said connection capacitor is a MOS capacitor that uses a p-channel.

Misawa discloses, a pixel capacitor (305 in fig. 15a/b) that is a p-channel MOS capacitor (col. 14, lines 61-68).

Misawa, Akimoto, Yamazaki and Stewart are analogous art because they are all from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the MOS capacitors taught by Misawa in the display device of Akimoto, Yamazaki and Stewart.

The motivation for doing so would have been to lower the number of manufacturing steps to form the display device (Misawa; col. 14, lines 55-60).

With respect to claim 8, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein each of said first switch, second switch, and said electro-luminescent element driving transistor is an n-channel transistor (fig. 6; also see para. 69).

Neither Akimoto nor Stewart expressly disclose, that said connection capacitor is a MOS capacitor that uses an n-channel.

Misawa discloses, a pixel capacitor (305 in fig. 15a/b) that is an n-channel MOS capacitor (col. 14, lines 61-68).

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the MOS capacitors taught by Misawa in the display device of Akimoto, Yamazaki and Stewart.

The motivation for doing so would have been to lower the number of manufacturing steps to form the display device (Misawa; col. 14, lines 55-60).

With respect to claims 16 and 19, as these claims are identical to previously rejected claims 5 and 8, respectively, these claims are rejected on the same merits shown above.

8. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Yamazaki et al. (US 6,417,896), Stewart et al. (US 5,952,789) and further in view of Akimoto et al. (US 6,670,936; hereinafter: Akimoto-'936).

With respect to claim 10, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein said signal line and said power supply line are disposed in parallel (clear from fig. 1 that 17 and 18 are parallel).

Neither Akimoto nor Yamazaki nor Stewart expressly disclose, forming the signal line and power supply by processing the same metallic wiring layer.

Akimoto-'936 discloses, a signal line (4 in fig. 1) and a power supply line (8 in fig. 1) are disposed in parallel (clear from fig. 1) and formed by processing the same metallic wiring layer (col. 6, line 62 – col. 7, line 7).

Akimoto, Yamazaki, Stewart and Akimoto-'936 are all analogous art because they are all form the same field of endeavor namely, pixel control circuitry and driving methods for image display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the signal and power supply lines of Akimoto, Yamazaki and Stewart on the same metallic wiring layer as taught by Akimoto-'936.

The motivation for doing so would have been to simplify the manufacturing process (Akimoto-'936; col. 7, lines 6-7).

With respect to claim 21, as this claim is identical to previously rejected claim 10, this claim is rejected on the same merits shown above.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Yamazaki et al. (US 6,417,896), Stewart et al. (US 5,952,789) and further in view of Miyajima et al. (US 6,812,912).

With respect to claim 22, Akimoto, Yamazaki and Stewart disclose, the image display device according to claim 21 (see above).

Neither Akimoto nor Yamazaki nor Stewart expressly disclose, that the connection capacitor is provided on the signal line in layers.

Miyajima discloses providing a capacitor (30 in fig. 14) that is provided on a signal line (data line; 22 in fig. 14) in layers (clear from fig. 15; also see col. 17, lines 41-48).

Akimoto, Yamazaki, Stewart and Miyajima are all analogous art because they are all form the same field of endeavor namely, pixel control circuitry for image display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the connection capacitor of Akimoto, Yamazaki and Stewart on the signal line in layers as taught by Miyajima.

The motivation for doing so would have been to increase the contrast and display quality of the image display device (Miyajima; col. 18, lines 38-39).

10. Claims 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Stewart et al. (US 5,952,789) and further in view of Misawa et al. (US 5,250,931).

With respect to claim 32, Akimoto discloses, an image display device (fig. 1), comprising:

a display part configured by a plurality of pixels (clear from fig. 1) each having an electro-luminescent element driven to illuminate according to a display signal voltage Vs (7 in fig. 1);

a signal line (17 in fig. 1) used to write said display signal voltage in said pixels (see write period in fig. 2);

a pixel selector (22 in fig. 1) for selecting a pixel from said plurality of pixels so as to write said display signal voltage therein through said signal line;

a display signal voltage generator (21 in fig. 1) for generating said display signal voltage;

an illuminating state controller (32, 9 in fig. 1) for controlling a selection of an illuminating state or non-illuminating state for each of said plurality of pixels at a time;

wherein one end of said electro-luminescent element provided in each said pixel is connected to a common power supply (common terminal connected to the element in fig. 1; also see end of para. 51) while the other end of said electro-luminescent element is selectively connected to a first source/drain electrode of an electro-luminescent element driving transistor (4 in fig. 1) through a first switch (9 in fig. 1) said transistor has a threshold voltage Vth,

a second source/drain electrode of said electro-luminescent element driving transistor is connected to a power supply line applied with a prescribed voltage (18 in fig. 1; para. 43), and

the gate of said electro-luminescent element driving transistor (4 in fig. 1) is connected to the signal line through a capacitance (2 in fig. 1) and selectively connected

to the first source/drain electrode of said electro-luminescent element driving transistor through a second switch (5 in fig. 1), and

when said illuminating state is selected, the first switch is fixed as ON, the second switch is fixed as OFF (see the waveforms for the light-on period in fig. 3), and a voltage that is lower than said prescribed voltage appears at the gate of said transistor (col. 6, lines 8-45),

a gate wiring forming the gate of said transistor is connected to the signal line directly through a capacitor element (fig. 1).

the electro-luminescent element driving transistor, the first switch and the second switch is formed with a p-type transistor (see fig. 4; para. 62),

a gate of the p-type transistor forming the capacitance is connected to the gate of the electro-luminescent driving transistor, and source and drain electrodes of the p-type transistor forming the capacitance are connected to the signal line (fig. 1), and

the signal voltage is set so as to become lower than a difference of the prescribed voltage of the power supply line minus the threshold voltage Vth (Akimoto's pixel circuit is identical to circuits presented by the Applicant, and furthermore Akimoto's disclosure details very similar operation to the current application (see col. 5, line 62 - col. 6, line 15). Therefore the voltage limitation on the gate of said transistor is seen as inherent in the operation of the pixel circuit disclosed by Akimoto).

Akimoto further discloses, a constant voltage supply, as evidenced by the signal line data during the write period in figure three. During an illumination period, Akimoto supplies a triangular signal amplitude as seen in figure three.

Akimoto does not expressly disclose supplying a constant voltage to each pixel during the illuminating state or that the constant voltage is lower than the prescribed voltage.

Stewart discloses, an image display device having an electro-luminescent element pixel circuit (610 in fig. 6; for example), wherein a constant voltage supply provides a constant voltage Vil (ground in fig. 4) to each of said plurality of pixels through said signal line (data line in fig. 6; D2 in fig 4) when said illuminating state is selected for a selected pixel (L1 in fig. 4; col. 6, lines 48-54), and that the constant voltage, Vil lower than said display signal voltage Vs (col. 6, lines 24-34) is applied to the signal line.

Stewart and Akimoto are analogous art because they are both from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the triangular signal amplitude of Akimoto with the constant supply voltage of Stewart.

The motivation for doing so would have been to ensure a high display quality over time (Stewart; col. 2, lines 1-4)

Neither Akimoto nor Stewart expressly disclose, that said connection capacitor is a MOS capacitor that uses a p-channel.

Misawa discloses, a pixel capacitor (305 in fig. 15a/b) that is a p-channel MOS capacitor (col. 14, lines 61-68).

Misawa, Akimoto and Stewart are analogous art because they are all from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the MOS capacitors taught by Misawa in the display device of Akimoto and Stewart.

The motivation for doing so would have been to lower the number of manufacturing steps to form the display device (Misawa; col. 14, lines 55-60).

With respect to claim 33, Akimoto discloses, an image display device (fig. 1), comprising:

a display part configured by a plurality of pixels (clear from fig. 1) each having an electro-luminescent element driven to illuminate according to a display signal voltage Vs (7 in fig. 1);

a signal line (17 in fig. 1) used to write said display signal voltage in said pixels (see write period in fig. 2);

a pixel selector (22 in fig. 1) for selecting a pixel from said plurality of pixels so as to write said display signal voltage therein through said signal line;

a display signal voltage generator (21 in fig. 1) for generating said display signal voltage;

an illuminating state controller (32, 9 in fig. 1) for controlling a selection of an illuminating state or non-illuminating state for each of said plurality of pixels at a time;

wherein one end of said electro-luminescent element provided in each said pixel is connected to a common power supply (common terminal connected to the element in fig. 1; also see end of para. 51) while the other end of said electro-luminescent element is selectively connected to a first source/drain electrode of an electro-luminescent element driving transistor (4 in fig. 1) through a first switch (9 in fig. 1) said transistor has a threshold voltage Vth,

a second source/drain electrode of said electro-luminescent element driving transistor is connected to a power supply line applied with a prescribed voltage (18 in fig. 1; para. 43), and

the gate of said electro-luminescent element driving transistor (4 in fig. 1) is connected to the signal line through a capacitance (2 in fig. 1) and selectively connected to the first source/drain electrode of said electro-luminescent element driving transistor through a second switch (5 in fig. 1), and

when said illuminating state is selected, the first switch is fixed as ON, the second switch is fixed as OFF (see the waveforms for the light-on period in fig. 3), and a voltage that is lower than said prescribed voltage appears at the gate of said transistor (col. 6, lines 8-45),

a gate wiring forming the gate of said transistor is connected to the signal line directly through a capacitor element (fig. 1).

the electro-luminescent element driving transistor, the first switch and the second switch is formed with a n-type transistor (see fig. 6; para. 69),

a gate of the n-type transistor forming the capacitance is connected to the gate of the electro-luminescent driving transistor, and source and drain electrodes of the n-type transistor forming the capacitance are connected to the signal line (fig. 1), and

the signal voltage is set so as to become lower than a sum of the prescribed voltage of the power supply line minus the threshold voltage Vth (Akimoto's pixel circuit is identical to circuits presented by the Applicant, and furthermore Akimoto's disclosure details very similar operation to the current application (see col. 5, line 62 - col. 6, line 15). Therefore the voltage limitation on the gate of said transistor is seen as inherent in the operation of the pixel circuit disclosed by Akimoto).

Akimoto further discloses, a constant voltage supply, as evidenced by the signal line data during the write period in figure three. During an illumination period, Akimoto supplies a triangular signal amplitude as seen in figure three.

Akimoto does not expressly disclose supplying a constant voltage to each pixel during the illuminating state or that the constant voltage is lower than the prescribed voltage.

Stewart discloses, an image display device having an electro-luminescent element pixel circuit (610 in fig. 6; for example), wherein a constant voltage supply provides a constant voltage Vil (ground in fig. 4) to each of said plurality of pixels through said signal line (data line in fig. 6; D2 in fig 4) when said illuminating state is selected for a selected pixel (L1 in fig. 4; col. 6, lines 48-54), and that the constant voltage, Vil lower than said display signal voltage Vs (col. 6, lines 24-34) is applied to the signal line.

Stewart and Akimoto are analogous art because they are both from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the triangular signal amplitude of Akimoto with the constant supply voltage of Stewart.

The motivation for doing so would have been to ensure a high display quality over time (Stewart; col. 2, lines 1-4)

Neither Akimoto nor Stewart expressly disclose, that said connection capacitor is a MOS capacitor that uses an n-channel.

Misawa discloses, a pixel capacitor (305 in fig. 15a/b) that is an n-channel MOS capacitor (col. 14, lines 61-68).

Misawa, Akimoto and Stewart are analogous art because they are all from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the MOS capacitors taught by Misawa in the display device of Akimoto and Stewart.

The motivation for doing so would have been to lower the number of manufacturing steps to form the display device (Misawa; col. 14, lines 55-60).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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